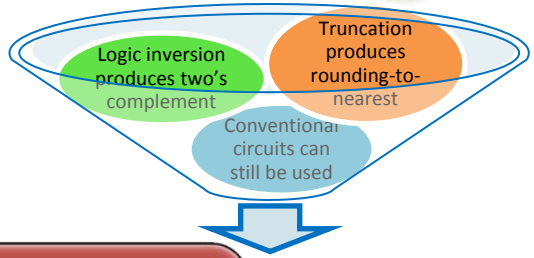
Advantages



HUB approach (patented)

Half Unit Biased

Hardware optimization of computation with real numbers

More Information
http://www.ac.uma.es/~hormigo/HUB.htm
Contact: fjhormigo@uma.es

KEEPING THE SAME PRECISION, IT SIMPLIFIES HARDWARE

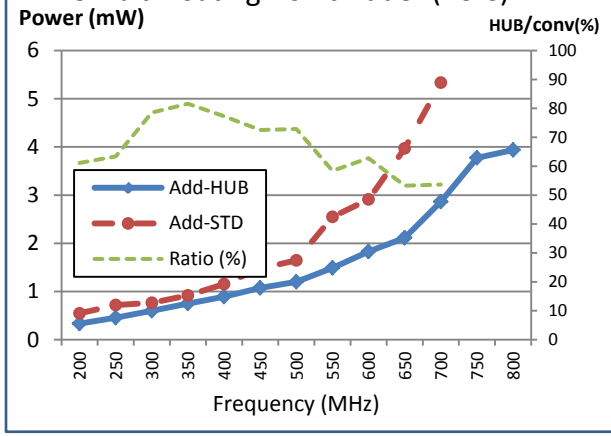
- **Less area** requirement
- **Less power** and **energy** consumption
- **Higher speed**

SLIGHT MODIFICATIONS AT LOGIC LEVEL

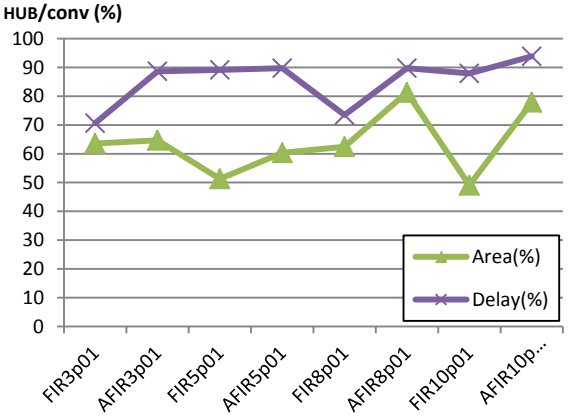
- Previous designs are **very easily adapted** to HUB
- Valid for **any technology (ASIC** or **FPGA)**

Optimization examples

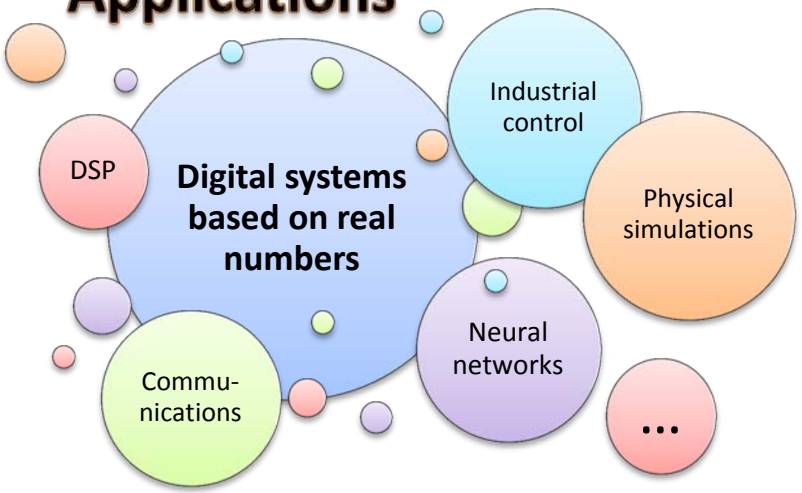
32-bit Floating-Point Adder (ASIC)



Fixed-Point FIR filters (FPGA)



Applications



Related publications

Basic Theory

J. Hormigo; J. Villalba, "New Formats for Computing with Real-Numbers under Round-to-Nearest," in IEEE Trans. on Computers, vol. 65, no. 7, pp. 2158-2168, July 2016
DOI: 10.1109/TC.2015.2479623

Fixed-point FIR Filters

J. Hormigo; J. Villalba, "Optimizing DSP circuits by a new family of arithmetic operators," 48th Asilomar Conference on Signals, Systems and Computers, Pacific Grove, CA, 2014, pp. 871-875.
DOI: 10.1109/ACSSC.2014.7094576

Floating-Point on FPGA

J.Hormigo; J. Villalba, "HUB-Floating-Point for improving FPGA implementations of DSP Applications," in IEEE Trans. on Circuits and Systems II, early access.
DOI: 10.1109/TCSII.2016.2563798

Fixed-point CORDIC

S. D. Muñoz; J. Hormigo, "Improving fixed-point implementation of QR decomposition by rounding-to-nearest," Int. Symp. on Consumer Electronics (ISCE), Madrid, 2015, pp. 1-2.
DOI: 10.1109/ISCE.2015.7177822

Floating-Point on ASIC

J. Hormigo; J. Villalba, "Measuring Improvement When Using HUB Formats to Implement Floating-Point Systems Under Round-to-Nearest," in IEEE Trans. on Very Large Scale Integration (VLSI) Systems, vol.24, no.6, pp.2369-2377, June 2016
DOI: 10.1109/TVLSI.2015.2502318

Half Precision Floating-Point

Hormigo ; J. Villalba, "Simplified floating-point units for high dynamic range image and video systems," 2015 Int. Symposium on Consumer Electronics (ISCE), Madrid, 2015, pp. 1-2.
DOI: 10.1109/ISCE.2015.7177797