Curriculum Vitae

Personal Information

Surname:	Hormigo-Aguilar
Firstname:	Francisco Javier
Place & date of birth:	Ronda (Malaga), April 3rd, 1973
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Education

- Ph.D. in Telecommunication Engineering, University of Malaga (Spain).
  Dissertation: “Architectures and algorithms for reliable computing of elementary functions” (”Arquitecturas y algoritmos para el calculo fiable de funciones elementales”).
  Graduation date: April, 2000.

- S.B.Sc.& M.Sc. in Telecommunication Engineering, University of Malaga (Spain).
  Thesis: “Neural Networks for Eigen-Analysis and Applications in Image Analysis” (RNA para CPA y su Aplicacion en el Analisis de Imagen”).
  Graduation date: November, 1996.

Professional Experience

- Associate Professor in Dept. Computer Architecture at University of Malaga (Spain) since August, 2001.

- Assistant Professor in Dept. Computer Architecture at University of Malaga (Spain) from October, 1999 to August, 2001.

- Assistant Researcher in Dept. Computer Architecture at University of Malaga (Spain) from January 1997 to October 1999, with support from Spanish Ministry of Education and Culture fellowship (Research Grant).

Research Projects as Chief Investigator

- “IP-CORE Design for Softaware Defined Radio Implementation in 4G Wireless comunication.” (Diseño de IP-cores para la implementación de Radio Definida por Software para comunicaciones inalámbricas 4G). Junta de Andalucia Grant, 2008-2012, 97000€.

- “Home Automation Allegro (Viability)”(Automatización residencial Allegro (viabilidad)), Business Contract, 2010-2011, 8100€

- “Embedded Control System COMET” (Módulo Controlador Empotrado COMET), 2008-2009, 17700€.

PhD Dissertations as supervisor

- Optimization of Hardware Resources for Convolution Computation in Digital Signal Processing by Carlos D. Moreno-Moreno, University of Córdoba, 2014.

- Efficient Use of Redundant Arithmetic in FPGA, by Manuel A. Ortiz-Lopez, University of Córdoba, 2014.

- Hardware Solutions for Range Reduction and Elementary Functions Computation, by Francisco J. Jaime-Rodriguez, University of Malaga, 2011.

- Application of On-line Arithmetic for Motion Estimation in MPEG, by Joaquin Olivares-Bueno, University of Córdoba, 2007.

- High Performance Computing Optimization by FPGA Accelerators, by Sergio Muñoz-Capo, University of Málaga, estimated 2016.

Stay in other research institutions

- He was with Dept. Electrical & Computer Engineering , University of Wisconsin-Madison , Wisconsin (USA), as research scholar , from July to September, in 2007.

- He was with ``Lehrstuhl fuer integrierte schaltungen'', Technical University of Munich, (Germany), as visiting research supported by DAAD grant, from March to June, in 2001.

- He was with Dept. Electrical Engineering & Computer Science of Lehigh University, Pennsylvania (USA), as visiting research, from May to July, in 1999.

- He was with Dept. Electrical Engineering & Computer Science of Lehigh University, Pennsylvania (USA), as visiting research, from April to June, in 1998.

- He was with Dept. Imaging & Vision (CSIC’s Research Institute of Optical), in 1996, with support from Spanish Research Council (Research Grant).

Others Merits

- Program Chair of the 23rd IEEE Symposium on Computer Arithmetic (ARITH23).
- Member of the Program Committee of the 22nd IEEE Symposium on Computer Arithmetic (ARITH22).
- Best paper Award at *31st IEEE International Conference on Computer Design (ICCD),* Oct. 2013:"Efficient Floating-Point Representation for Balanced Codes for FPGA Devices".
- Referee for many international journals and conferences, such as *IEEE Trans. on Computers, IEEE Trans. on Circuits and Systems for Video Technology,* as *IEEE Trans. on Multimedia, IEEE Trans. on Signal Processing, IET Circuits, Devices & Systems, EURASIP Journal on Advances in Signal Processing and others.*
- Researcher on several Research Projects supported by the Spanish Government since 1997.

Research Publications

PATENTS

-Hormigo, Javier; Villalba-Moreno, Julio. Multiplicadores coma flotante y conversores asociados, ES2546895B2, 2015.

-Hormigo, Javier; Villalba-Moreno, Julio. Dispositivos coma flotante y conversores, ES2546898B2, 2015.

-Hormigo, Javier; Villalba-Moreno, Julio. Sumadores coma flotante y conversores, ES2546916B2, 2015.

-Hormigo, Javier; Villalba-Moreno, Julio. Unidades aritméticas en coma fija y conversores asociados, ES2546915B2, 2015.

-Hormigo, Javier; Villalba-Moreno, Julio. Dispositivos para operaciones de multiplicación-suma fusionadas en coma flotante y conversores asociados, ES2546899B2, 2015.

-Hormigo, Javier; Caffarena-Fernandez, Gabriel; García, J. Manuel. Sistema y método para la optimización de anchos de palabra de circuitos digitales mediante simulaciones bit-true, ES2562072A1, 2016.

JOURNAL PAPERS

- J. Hormigo; J. Villalba, "HUB-Floating-Point for improving FPGA implementations of DSP Applications," in IEEE Transactions on Circuits and Systems II: Express Briefs , vol.PP, no.99, pp.1-1. IEEE Early access.

- J. Hormigo and J. Villalba, "New Formats for Computing with Real-Numbers under Round-to-Nearest," in IEEE Transactions on Computers, vol. 65, no. 7, pp. 2158-2168, July 2016.

- J. Hormigo and J. Villalba, "Measuring Improvement When Using HUB Formats to Implement Floating-Point Systems Under Round-to-Nearest," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 24, no. 6, pp. 2369-2377, June 2016.

- S. D. Muñoz and J. Hormigo, "High-Throughput FPGA Implementation of QR Decomposition," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 62, no. 9, pp. 861-865, Sept. 2015.

- Hormigo, J. ; Caffarena, G. ; Oliver, J.; Boemo, E., “Self-reconfigurable Constant Multiplier for FPGA”. *ACM Transactions on Reconfigurable Technology and Systems* 6 - 3:14, 2013.

- Hormigo, J.; Villalba, J.; Zapata, E.L., "Multioperand Redundant Adders on FPGAs", *IEEE Transactions on Computers*, vol.62, no.10, pp.2013,2025, Oct. 2013.

- Villalba, J.; Lang, T.; Hormigo, J., "Radix-2 Multioperand and Multiformat Streaming Online Addition", *IEEE Transactions on Computers*, vol.61, no.6, pp.790,803, June 2012.

- Gonzalez-Navarro, S., Hormigo, J., Schulte, M.J. “A study of decimal left shifters for binary numbers”, *Information and Computation*, 216, pp. 47-56, 2012.

- Moreno, C.D., Martínez, P., Bellido, F.J., Hormigo, J., Ortiz, M.A., Quiles, F.J. “Convolution computation in FPGA based on carry-save adders and circular buffers”, *Lecture Notes of the Institute for Computer Sciences, Social-Informatics and Telecommunications Engineering*, 82 LNICST, pp. 237-248, 2012.

- Jaime, F.J.; Sánchez, M.A.; Hormigo, J.; Villalba, J.; Zapata, E.L., "High-Speed Algorithms and Architectures for Range Reduction Computation,", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol.19, no.3, pp.512,516, March 2011.

-Jaime, F.J.; Sánchez, M.A.; Hormigo, J.; Villalba, J.; Zapata, E.L., "Enhanced Scaling-Free CORDIC," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol.57, no.7, pp.1654,1662, July 2010.

- Jaime, F.J., Villalba, J., Hormigo, J., Zapata, E.L.”Pipelined architecture for additive range reduction”, Journal of Signal Processing Systems, 53 (1-2 SPEC. ISS.), pp. 103-112, 2008.

- J. Olivares, J. Hormigo, J. Villalba, I. Benavides and E. L. Zapata, "SAD computation based on online arithmetic for motion estimation," Microprocessors & Microsystems, vol. 30, pp. 250-258, 2006.

- J. Hormigo and G. Cristóbal, "Image segmentation using the Wigner-Ville distribution," Advances Imaging Electron Phys., vol. 131, pp. 65-80, 2004.

- J. Hormigo, J. Villalba and E. L. Zapata, "CORDIC Processor for Variable-Precision Interval Arithmetic," J VLSI Signal Process Syst Signal Image Video Technol, vol. 37, pp. 21-39, 2004.

- Gabriel Cristobal and Javier Hormigo,"Texture Segmentation Through Eigen-Analysis of the Pseudo-Wigner Distribution", Pattern Recognition Letters, vol.20, no. 3, pp. 337–345, March, 1999.

- Javier Hormigo and Gabriel Cristobal, "High Resolution Spectral Analysis of Images Using the Pseudo-Wigner Distribution", IEEE Transactions on Signal Processing, vol. 46, no. 6, pp. 1757–1763, July 1998.

REFEREED CONFERENCE PAPERS

- S. D. Muñoz and J. Hormigo, "Improving fixed-point implementation of QR decomposition by rounding-to-nearest," 2015 International Symposium on Consumer Electronics (ISCE), Madrid, 2015, pp. 1-2.

- J. Hormigo and J. Villalba, "Simplified floating-point units for high dynamic range image and video systems," 2015 International Symposium on Consumer Electronics (ISCE), Madrid, 2015, pp. 1-2.

- Javier Hormigo, Julio Villalba, "Optimizing DSP Circuits by a New Family of Arithmetic Operators", 48th Annual Asilomar Conference on Signals, Systems, and Computers, Nov 2014.

- Julio Villalba, Javier Hormigo, Mario Gonzalez-Peñalver, Francisco Corbera and Emilio L. Zapata, "Efficient Floating-Point Representation for Balanced Codes for FPGA Devices", *31st IEEE International Conference on Computer Design (ICCD),* Oct. 2013. **Best paper Award**.

- Muñoz-Capo, Sergio; Hormigo, Javier; López-Zapata, Emilio "FGPA implementation of QR decomposition for medium size matrices", *XXVII Conference on Design of Circuits and Integrated Systems,* Nov. 2012.

- Quiles, F.J.; Ortiz, M.; Brox, M.; Moreno, C.D.; Hormigo, J.; Villalba, J., "UCORE: Reconfigurable Platform for Educational Purposes," *Reconfigurable Computing and FPGAs (ReConFig), 2010 International Conference on* , vol., no., pp.109,114, 13-15 Dec. 2010.

- Murugappan Senthilvelan; Hormigo, J.; Joon Hwa Chun; Sima, M.; Iancu, D.; Schulte, M.; Glossner, J., "CORDIC-based LMMSE equalizer for Software Defined Radio,"

Embedded Computer Systems (SAMOS), 2010 International Conference on , vol., no., pp.301,308, 19-22 July 2010

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- Moreno, C.D., Quiles, F.J., Ortiz, M.A., Brox, M., Hormigo, J., Villalba, J., Zapata, E.L.,"Efficient mapping on FPGA of convolution computation based on combined CSA-CPA accumulator", 16th IEEE International Conference on Electronics, Circuits and Systems, ICECS 2009 , pp. 419-422. 2009

- Ortiz, M., Quiles, F., Hormigo, J., Jaime, F.J., Villalba, J., Zapata, E.L. "Efficient implementation of carry-save adders in FPGAs", Proceedings of the International Conference on Application-Specific Systems, Architectures and Processors, pp. 207-210. 2009

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- Manuel Hernández Calviño, José Ignacio Benavides Benítez, Sergio R. Geninatti, Francisco Javier Hórmigo, Julio Villalba Moreno, "Hardware Accelerators for the Microblaze Software Embedded Processor", *III Southern Conference on Programmable Logic (SPL)*, Feb. 2007.

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- F.J. Jaime, J. Villalba, J. Hormigo y E.L. Zapata,"Pipelined Architecture for double residue based generator", 17th IEEE International Conference on Application specific Systems, Architectures and Processors (ASAP 2006), pp. 145-150,Colorado, USA 2006.

- Joaquín Olivares, Ignacio Benavides, Javier Hormigo and Julio Villalba," Fast Full-Search block matching Algorithm Motion Estimation Alternatives in FPGA", The International Conference on Field Programmable Logic and Applications (FPL 06) Madrid, Spain, 2006.

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- Javier Hormigo, Julio Villalba and Michael J. Schulte, ”Hardware algorithm for Variable-Precision Logarithm”, Proc. 12th International Conference on Application-specific Systems, Architectures and Processors, pp. 215-224, Boston (USA), 10-12 July, 2000.

- J. Villalba, J. Hormigo, M.A. Gonzalez and E.L. Zapata, “MMX architecture extension to support the rotation operation”, IEEE International Conference on Multimedia and Expo, New York (USA), 30 July -2 August, 2000.

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- J. Hormigo, J. Villalba and E.L. Zapata, ”Interval sine and Cosine Functions Computation Based on Variable–Precision CORDIC Algorithm ”, 14th IEEE Symposium on Computer Arithmetic(ARITH’14), pp. 186–193, Adelaide(Australia), 14–16 April, 1999.

- J. Hormigo, J. Villalba and E.L. Zapata,”Arithmetic Unit for the Computation of Interval Elementary Functions”. Proceedings 25th EUROMICRO Conference, Workshop on Digital System Design, Milan (Italy), 8–10 September, 1999.

- M. G. Peñalver, J. Hormigo, J. Villalba and E.Saez and E. L. Zapata, ”FPGA implementation of a CORDIC processor with reduced number of iterations”. Proceedings

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- J. Hormigo, J. Villalba and E.L. Zapata, "CORDIC Algorithm with Digits Skipping", 32th Asilomar Conference on Signals, Systems, and Computers, pp. 194–196, Monterey (USA), 1–4 November, 1998.

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BOOK CHAPTERS

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- Javier Hormigo, Julio Villalba and Emilio L. Zapata, Developments in Reliable Computing (T. Csendes ed.), "A Hardware Approach to Interval Sine and Cosine Computation", pp 31–41, Kluwer Academic Publishers, 1999.